WHAT IS CLAIMED IS:

1. A pulse width modulation (PWM) signal generator comprising a signal generating device for generating one or two pulses which have a pulse width or a total pulse width corresponding to a value represented by a pulse code modulation digital signal and which have a symmetric positional relationship with respect to the position of one half of a predetermined length, as a first pulse width modulation signal, wherein

said signal generating device includes a PCM (pulse code modulation)-PWM converter which generates a first pulse and a second pulse in accordance with the value represented by the digital signal, and a difference detector which outputs the difference between the first pulse and the second pulse, as the first pulse width modulation signal, and

when the value represented by the digital signal is zero, the first pulse and the second pulse are equal to each other in pulse width, and when the value represented by the digital signal changes by one, one of the first and second pulses does not change in pulse width and the other of the first and second pulses changes in pulse width by two slots.

2. The PWM signal generator according to claim 1, further comprising an odd-number detector which detects that the value represented by the digital signal represents an odd-number, wherein when the value represented by the digital signal represents an odd-number, said signal generating device alternately generates the first pulse width modulation

signal, and a second pulse width modulation signal comprising two pulses having a total pulse width corresponding to the odd value and placed in a symmetric positional relationship to the one pulse or two pulses of the first pulse width modulation signal with respect to the positions of 1/4 and 3/4 of the predetermined length.

3. The PWM signal generator according to claim 2, wherein a slot value LE at a leading edge and a slot value TE at a trailing edge of the first pulse are calculated by:

LE = SLOT/2 - (INT)(PCMOFST/2)

TE = SLOT/2 + (INT)(PCMOFST/2)

when the first pulse width modulation signal is generated, where SLOT is the number of slots of the predetermined length, PCMOFST is a value of the digital signal offset by SLOT/2, and INT is a rounding operation;

a slot value LE at a leading edge position and a slot value TE at a trailing edge position of the second pulse are calculated by:

LE = (INT)((PCMOFST+1)/2)

TE = SLOT - (INT)((PCMOFST+1)/2)

when the first pulse width modulation signal is generated;

the slot value LE at the leading edge position and the slot value TE at the trailing edge position of the first pulse are calculated by:

LE = SLOT/2 - (INT)((PCMOFST+1)/2)

TE = SLOT/2 + (INT)((PCMOFST+1)/2)

when the second pulse width modulation signal is generated;

and

the slot value LE at the leading edge position and the slot value TE at the trailing edge position of the second pulse are calculated by:

LE = (INT)((PCMOFST-1)/2)

TE = SLOT - (INT)((PCMOFST-1)/2)

when the second pulse width modulation signal is generated.

4. The PWM signal generator according to claim 2, wherein said odd-number detector determines an odd-number or an even-number in accordance with the value at the least significant bit of the digital signal.

5. The PWM signal generator according to claim 2, wherein said signal generating device includes:

a first signal generator which generates the first pulse width modulation signal;

a second signal generator which generates the second pulse width modulation signal; and

a selector which outputs the first pulse width modulation signal when the value represented by the digital signal represents an even-number, and alternately outputs the first pulse width modulation signal and the second pulse width modulation signal when the value represented by the digital signal represents an odd-number.

6. A PWM signal generating method for generating one or two pulses having a pulse width or a total pulse width corresponding to a value represented by a pulse code modulation digital signal and placed in a symmetric

positional relationship with respect to the position of one half of a predetermined length, as a first pulse width modulation signal, the method comprising the steps of:

generating a first pulse and a second pulse in accordance with a value represented by the digital signal;

outputting the difference between the first pulse and the second pulse, as the first pulse width modulation signal; and

controlling the first pulse and the second pulse so that when the value represented by the digital signal is zero, the first pulse and the second pulse are equal to each other in pulse width, and when the value represented by the digital signal changes by one, one of the first and second pulses does not change in pulse width and the other of the first and second pulses changes in pulse width by two slots.

7. A PWM signal generating method for generating one or two pulses having a pulse width or a total pulse width corresponding to a value represented by a pulse code modulation digital signal and placed in a symmetric positional relationship with respect to the position of one half of a predetermined length, as a first pulse width modulation signal, the method comprising the steps of:

controlling the first pulse and the second pulse so that when the value represented by the digital signal is zero, the first pulse and the second pulse are equal to each other in pulse width, and when the value represented by the digital signal changes by one, one of the first and second pulses

does not change in pulse width and the other of the first and second pulses changes in pulse width by two slots;

detecting that a value represented by the digital signal is an odd-number; and

when the value represented by the digital signal is an odd-number, generating the first pulse width modulation signal and a second pulse width modulation signal, alternately, said second pulse width modulation signal comprising two pulses having a total pulse width corresponding to the odd value and placed in a symmetric positional relationship to the one pulse or two pulses of the first pulse width modulation signal with respect to the positions of 1/4 and 3/4 of the predetermined length.

8. A digital-to-analog converter comprising:

an oversampling circuit which oversamples an input pulse code modulation digital signal;

a delta-sigma modulator which decreases the number of quantization bits of an output digital signal of said oversampling circuit;

a PWM signal generator which generates one or two pulses having a pulse width or a total pulse width corresponding to a value represented by an output digital signal of said delta-sigma modulator and placed in a symmetric positional relationship with respect to the position of one half of a predetermined length, as a first pulse width modulation signal; and

a low pass filter which outputs a low band component of

the first pulse width modulation signal,

wherein said PWM signal generator includes a PCM-PWM converter which generates a first pulse and a second pulse in accordance with the value represented by the output digital signal of said delta-sigma modulator, and a difference detector which outputs the difference between the first pulse and the second pulse, as the first pulse width modulation signal; and

when the value represented by the output digital signal of said delta-sigma modulator is zero, the first pulse and the second pulse are equal to each other in pulse width, and when the value represented by the output digital signal of said delta-sigma modulator changes by one, one of the first and second pulses does not change in pulse width and the other of the first and second pulses changes in pulse width by two slots.

9. A digital amplifier comprising:

an oversampling circuit which oversamples a pulse code modulation input digital signal;

a digital volume which changes a gain indicated by an output digital signal of said oversampling circuit;

a delta-sigma modulator which decreases the number of quantization bits of an output digital signal of said digital volume;

a PWM signal generator which generates one or two pulses having a pulse width or a total pulse width corresponding to a value represented by an output digital signal of said

delta-sigma modulator and placed in a symmetric positional relationship with respect to the position of one half of a predetermined length, as a first pulse width modulation signal; and

a low pass filter which outputs a low band component of the first pulse width modulation signal,

wherein said PWM signal generator includes a PCM-PWM converter which generates a first pulse and a second pulse in accordance with the value represented by the output digital signal of said delta-sigma modulator, and a difference detector which outputs the difference between the first pulse and the second pulse, as the first pulse width modulation signal; and

when the value represented by the output digital signal of said delta-sigma modulator is zero, the first pulse and the second pulse are equal to each other in pulse width, and when the value represented by the output digital signal of said delta-sigma modulator changes by one, one of the first and second pulses does not change in pulse width and the other of the first and second pulses changes in pulse width by two slots.